```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 2024/08/13 16:02:40
// Design Name:
// Module Name: tb_ClkGen
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module tb_ClkGen(

    );

    // Declaration Signal
    reg DATA, SCLK, SET, RESET;
    //reg CLK;
    wire OUT, led2;
    wire [7:0] LUTLO_W;
    wire [23:0] LAO_W, SUMLO_W;

    parameter clk = 12.000000;
    parameter STEP = (1 / clk *1000) * 5;

    reg GCLK = 1'b0;
    always #(((1/clk) / 2.0) *1000) GCLK = ~GCLK;


    // Call Test Module
    ClkGen ClkGen(
       DATA,
       SCLK,
       SET,
       RESET,
       GCLK,
       OUT,
       led2
       //LUTLO_W,
       //LAO_W,
       //SUMLO_W
    );

    // Input Condition
    integer i;

    task WrFreq(
        input [23:0]    SRData
        );
        begin
        for (i = 0; i < 24; i = i + 1) begin
            DATA = SRData[0];
            SRData = SRData >> 1;
            #STEP
            SCLK = 1;
            #STEP
            SCLK = 0;
        end
        #STEP
        SET = 1;
        #STEP
        SET = 0;
        end
    endtask

```

```
77        //test
78        initial begin
79
80            $display("start...");
81
82            RESET = 0;
83            #STEP
84            RESET = 1;
85            #STEP
86            #(STEP * 150)
87            SET = 0;
88            SCLK = 0;
89            #STEP
90
91            //3MHz
92            //WrFreq(4194304);
93            //1KHz
94            //WrFreq(1398);
95            WrFreq(1000*2);      // 1KHz
96
97            #(STEP * 1000000000)   $finish;
98
99        end
100
101   endmodule
```